International Journal of Recent Research in Science, Engineering and Technology

Vol. 1, Issue 1, April 2015

A PERFORMANCE COMPARISON OF LOW POWER LFSR STRUCTURES

Nithya. R[1], Paviya. M[1], Poornimadevi.A[1], Selvaraj Ravi[2]

Final year ECE, Global Institute of Engineering and technology, Vellore, Tamilnadu, India[1]

Assistant Professor, Global Institute of Engineering and technology, Vellore, Tamilnadu, India[2]

ABSTRACT: Testing is an important process in all electronic systems and it plays a vital role in electronic systems that are used in avionics, space, and safety critical applications. Apart from manufacturing test, which is carried out immediately after the chip is fabricated, periodic testing is also becoming important in these types of applications. Built-in Self Test (BIST) provides economical and reliable solution under this condition. However, silicon area due to redundant BIST circuitry represents a significant percentage of overall area of the chip. Also the power dissipation during test mode is about twice than that of the normal mode operation of the chip. To alleviate these problems several low power LFSR structures are proposed in various literatures over the past decade. This paper presents a comparison of various low power LFSR architectures presented in these research articles.

Keyword: Testing of VLSI, Built-in self test, Linear Feedback Shift Register, gated Clock LFSR, Dual speed LFSR, Bit swapping LFSR, Weighted LFSR.

I. Introduction

Tests are run on the first batch of chips that return from fabrication. Testing helps to sell good chips to the customer and prevents the problems that arise after selling faulty chips [1]. Testing verifies the functionality and performance of the fabricated chip. Testing a chip can occur at various levels such as Wafer level, packaged chip level, system level, and in the field. Dust particles and small imperfections in starting material, process variation due to environment effects, or mask misalignments, etc., can result in bridged connections or missing features in the fabricated chip. These imperfections results in defects in a chip, and the physical model used to represent its effect is called as fault. The task of testing a faulty chip is to verify correct functionality by applying known set of input patterns and verifying its output with the expected good response [2]. However, due to increased chip density and complex circuitry makes the testing process becomes extremely complex and often very time consuming. A widely accepted approach to deal with the testing problem at the chip level is to incorporate Built-In-Self-Test (BIST) capability inside a chip. BIST is a technique that enables an IC to test itself. Typical test environment for full adder circuit using BIST technique is shown in figure 1. In order to test the full adder circuit, its output response for each

International Journal of Recent Research in Science, Engineering and Technology

Vol. 1, Issue 1, April 2015

binary input combination must match with the expected good response, which is stored in memory. The size of the memory required to test the full adder circuit is 8 x 2 (i.e, Eight locations and each location stores two bit data).

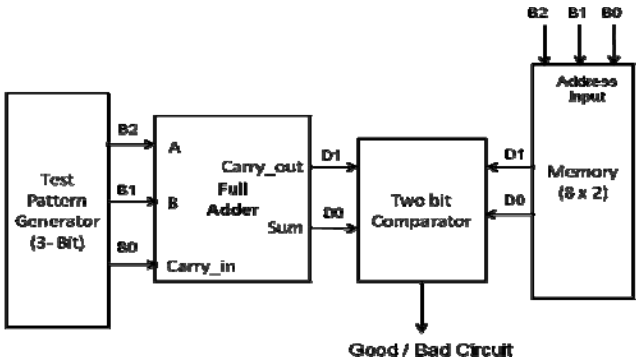


Figure1. Test environment for Full adder circuit

The eight memory location indicates eight possible binary input combinations and the size of each location is decided by the number of bits in the output. The test pattern generator can be a three bit binary counter that generates all eight (2^3) possible binary combinations or it may be an LFSR that generates seven (2^3-1) binary combinations. When the entire set-up is available within the integrated circuit (also called chip) and test process is carried out automatically then such a technique is called Built-in self test (BIST). BIST reduces test and maintenance costs for an IC by eliminating the need for expensive test equipment and by allowing fast location of failed ICs in a system. Despite all of these advantages, BIST has seen limited use in industry because of area and performance overhead and increased design time.

The organization of this paper is as follows: Section 2 presents literature review on low power testing methods. Section 3 presents the details of the LFSR structures considered in this work. Section 4 and 5 presents the simulation results and conclusion, respectively.

II. Literature Review

Testing of a system is an experiment on the fabricated chip to ascertain that it behaves correctly. The fundamental testing concepts and various types of testing are presented in [2]. A low power test pattern generator based on modified clock scheme is presented in [3]. A survey on low power testing techniques for test pattern generation and test application process steps of BIST is presented in [4]. Clock signal is major source of power consumption in synchronous sequential circuits and clock gating technique to reduce power consumption is presented in [5]. A combined approach for low power test pattern generation using binary counter, gray code counter, and LFSR is presented in [6]. Reducing test power consumption by using Dual Speed (slow and normal speed) LFSR (DS-LFSR)

International Journal of Recent Research in Science, Engineering and Technology

Vol. 1, Issue 1, April 2015

is presented in [7]. This paper presents some of the popular LFSR architectures and the corresponding simulation results.

III. Low power LFSR Structures

Power consumption in digital circuits is contributed by two major components, namely

(i) Static power consumption
(ii) Dynamic power consumption

The static power consumption is due to leakage current in the circuit during steady state conditions. The dynamic power consumption occurs when there is switching activity in the circuit and is represented by the following mathematical expression:

$$P_{Dyn} = 0.5\, V_{DD}^2\, E\,(sw)\, f_{clk}\, C_L \quad \ldots . \quad (1)$$

Where,

V_{DD} - Supply voltage
E (sw) - Average number of output transitions for one clock period (1/ fclk)
f_{clk} - Clock frequency
C_L - Physical capacitance at the output of the gate.

Reducing supply voltage, and clock frequency affects the circuit performance. Reducing Load capacitance is mainly depends on fabrication technology. Hence, the power consumption can be reduced by reducing the average number of switching transients which does not alter the functionality of the circuit [12, 13].

A linear feedback shift register (LFSR) is used in a variety of applications such as Built-in self test (BIST), cryptography, error correction code, and in the field of communication for generating pseudo-noise sequences. Due to the versatile nature of LFSR, various low-power architectures have been proposed. The following sections of the paper describe the hardware implementation of normal LFSR and four low-power LFSR architectures.

3.1 Normal LFSR:

Usually a linear feedback shift register (LFSR) is used to generate the pseudo random patterns to be used as test vectors in testing the circuit under test (CUT). LFSR is an arrangement of flip flops, in which some of the inputs and outputs are added in modulo-2 addition to provide the input to the register. The Overall output of LFSR acts as a Test Pattern. A 4-Bit LFSR structure is shown in fig. 2. In this structure the feedback from the last FF is the input to the first FF of the shift register and all the taps are XORed with the feedback to modify the input to the next FF in the shift register.

International Journal of Recent Research in Science, Engineering and Technology

Vol. 1, Issue 1, April 2015

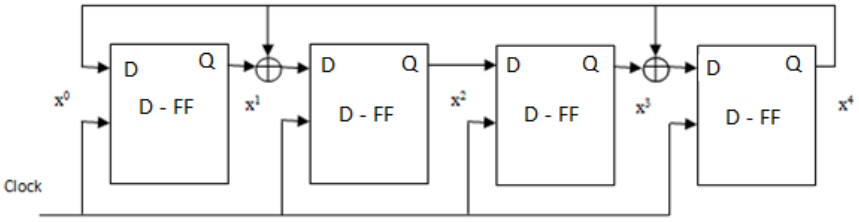


Figure 2. A 4-bit LFSR

The feedback connections or tapping points in an LFSR is represented by a polynomial function called characteristics polynomial. The feedback connections decide the number of possible binary combinations in the flip-flops, called length of the sequence.

3.2 Gated Clock LFSR

An LFSR is a shift-register where the output bit is an XOR function of some of the flip-flop output bits. At each clock cycle, the output bit of each flip-flop is shifted sequentially to the input of the next flip-flop. The output bits of the flip-flops are also used for XOR functions in the feedback loop. All the flip-flops change their states and are active at each clock cycle resulting in high power consumption. Gated clock LFSR uses D-flip-flops with gated clock structure. The unwanted switching transients in the D flip-flop is eliminated by introducing XOR-AND structure at the clock input of the flip-flop as shown in fig. 3. This structure enables the clock only when the present state and D input are different i.e., only when the state change needs to occur [13].

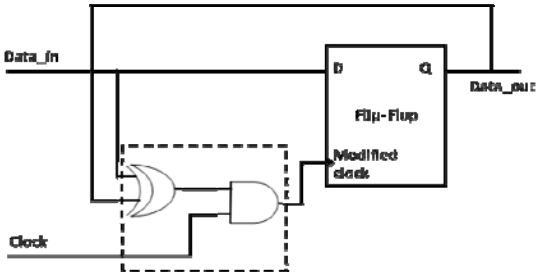


Figure 3. Gated clock D flip-flop

The functionality of gated scan flip-flop is described in Table 1. It can be observed from the table that the modified clock is activated (logic 1) only when the data input and present state are different.

International Journal of Recent Research in Science, Engineering and Technology

Vol. 1, Issue 1, April 2015

Input D	Present State, Q(t)	Next State, Q(t+1)	Clock	Modified clock
0	0	0	1	0
0	1	0	1	1
1	0	1	1	1
1	1	1	1	0

Table 1 D Flip-flop operation with modified clock

According to table 1, the clock is disabled two times; hence the power consumption is reduced up to 50 %. Since the added clock gating circuitry (XOR_AND) structure consumes some amount of power, the average power consumption in the overall LFSR structure can be saved up to 25%.

3.3 Bit swapping LFSR

The Bit-Swapping LFSR (BS-LFSR), is composed of an LFSR and 'n' number of 2 × 1multiplexers, where n is the size of the LFSR. The multiplexers in the output lines of the LFSR select the bit swapping operation. A 3- stage Bit swapping LFSR is as shown in figure 4.

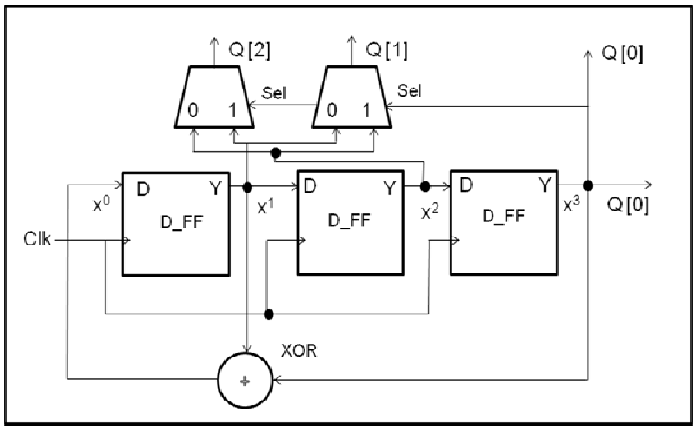


Figure 4 Three stage Bit swapping LFSR

The number of multiplexers increases as that of the size of the LFSR. However, the important aspect of selection of this approach is that multiplexers are very commonly available resources in all types of FPGA structures. This can

International Journal of Recent Research in Science, Engineering and Technology

Vol. 1, Issue 1, April 2015

be utilized for reducing the number of switching transients in the LFSR output which in turn reduces the power consumption. It is observed that the total number of switching transients for a complete cycle, the normal LFSR takes 12 transients while the BS LFSR takes only 10 transients. As the power consumption in a digital circuit is directly proportional to the number of switching transients (According Equation 1), the BSLFSR approach reduces the power consumption in the circuit.

3.4 Dual speed LFSR:

Another LFSR structure to reduce overall switching activities in the circuit under test is as shown in figure 5. This technique is called dual-speed LFSR (DS-LFSR), as it uses two different-speed LFSRs to control those inputs that have elevated transition densities [9, 11]. This technique eliminates unwanted power consumption by applying test patterns at slow speed for verifying the functionality of slow operated modules in system.

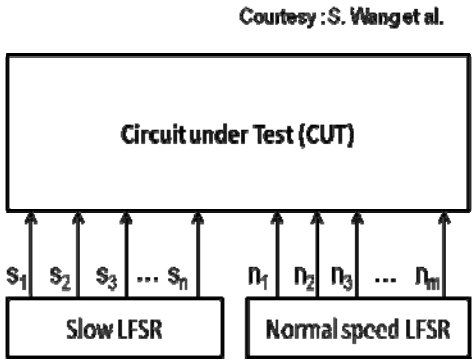


Figure 5 Dual speed LFSR (DS-LFSR)

3.5 Weighted LFSR

The random pattern resistant faults in the circuit under test (CUT) can be detected using deterministic test pattern generation technique. Weighted LFSR is one such technique in which test patterns are generated with required weight i.e., number of 1's in the test pattern [8, 10, 14]. This structure is constructed from the normal LFSR structure with additional number of AND gates (which reduces number of 1's in the output pattern) and OR gates (which increases number of 1's in the output pattern as shown in figure 6.

International Journal of Recent Research in Science, Engineering and Technology

Vol. 1, Issue 1, April 2015

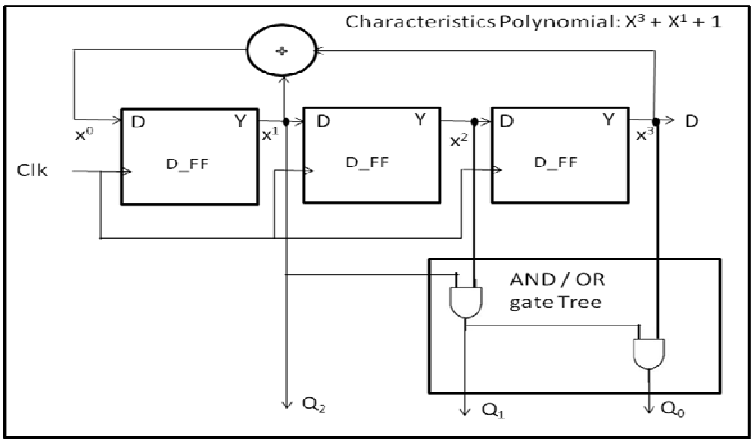
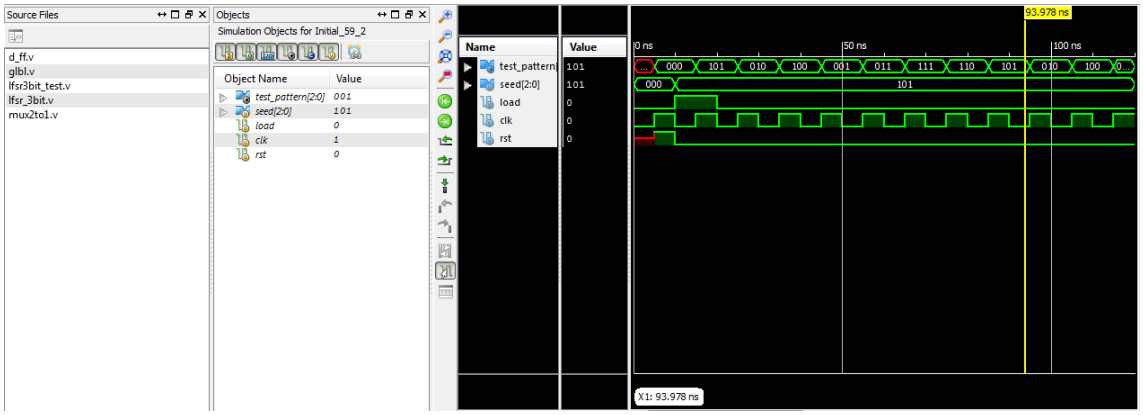


Figure 6 Weighted LFSR (3- Bit)

IV. Simulation Results

This section presents the simulation results for normal/conventional LFSR, Bit swapping LFSR, and weighted LFSR for four different weights. The weighted LFSR uses AND / OR gate tree to generate the weights of 0.25, 0.75, 0.125, and 0.875. The conventional LFSR generates the binary sequence with 0.5 weight, i.e., equal number of 1's and 0's.

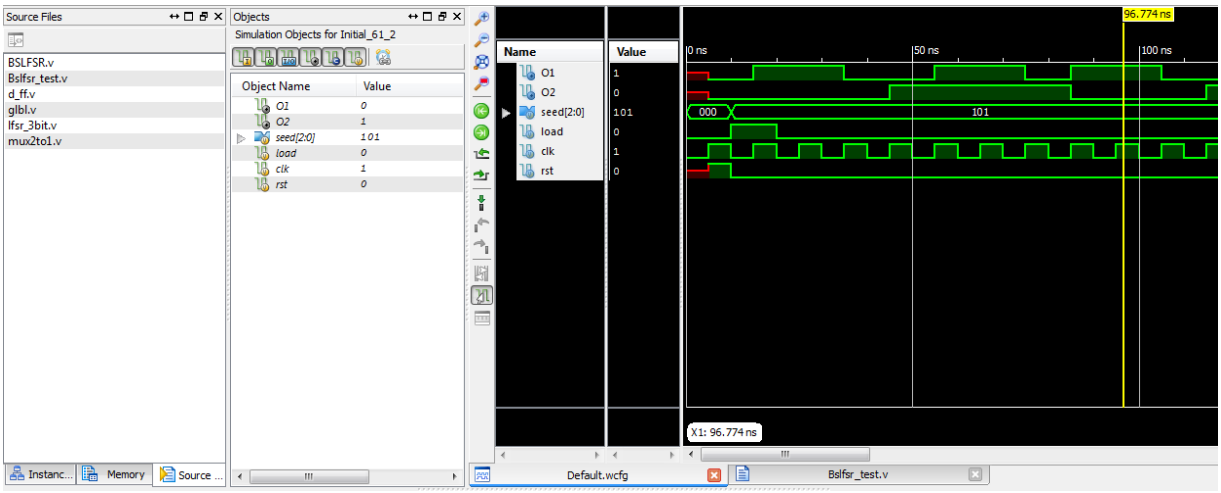
Normal LFSR (3-Bit)



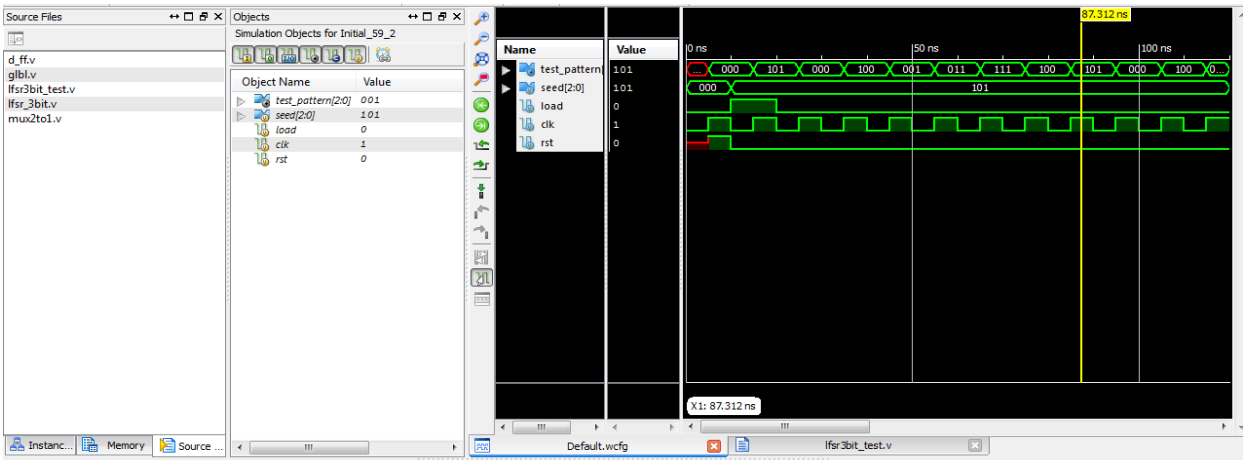
International Journal of Recent Research in Science, Engineering and Technology

Vol. 1, Issue 1, April 2015

Bit Swapping LFSR (3 - Bit)



Weighted LFSR (With Probability of Number of 1s = 0.25)



International Journal of Recent Research in Science, Engineering and Technology

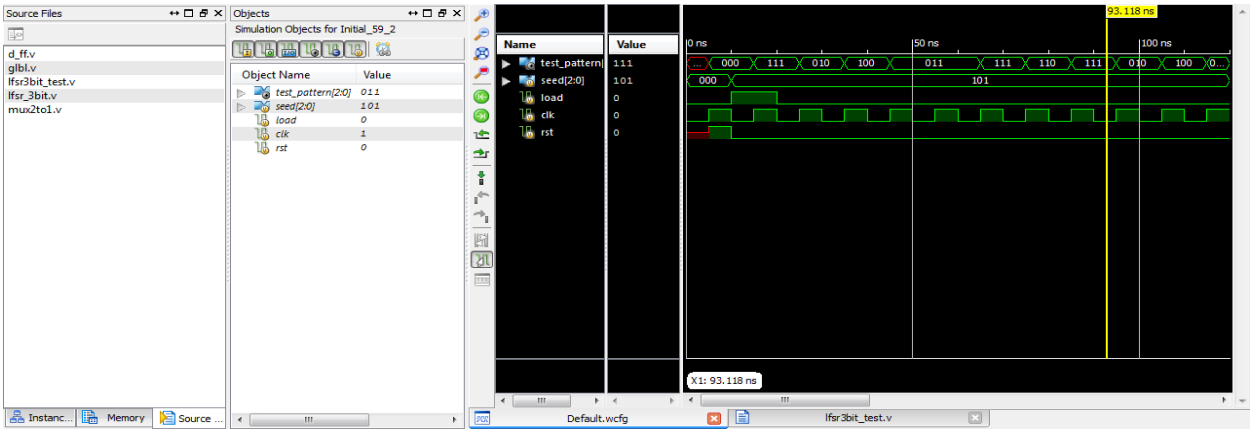
Vol. 1, Issue 1, April 2015

Test Pattern Sequence:

S. No	Q[2]	Q[1]	Q[0]
1	1	0	1
2	0	0	0
3	1	0	0
4	0	0	1
5	0	1	1
6	1	1	1
7	1	0	0
8	1	0	1

Note: Pattern 110 is replaced by 000. Seed Value: 101

Weighted LFSR (With Probability of Number of 1s = 0.75)



International Journal of Recent Research in Science, Engineering and Technology

Vol. 1, Issue 1, April 2015

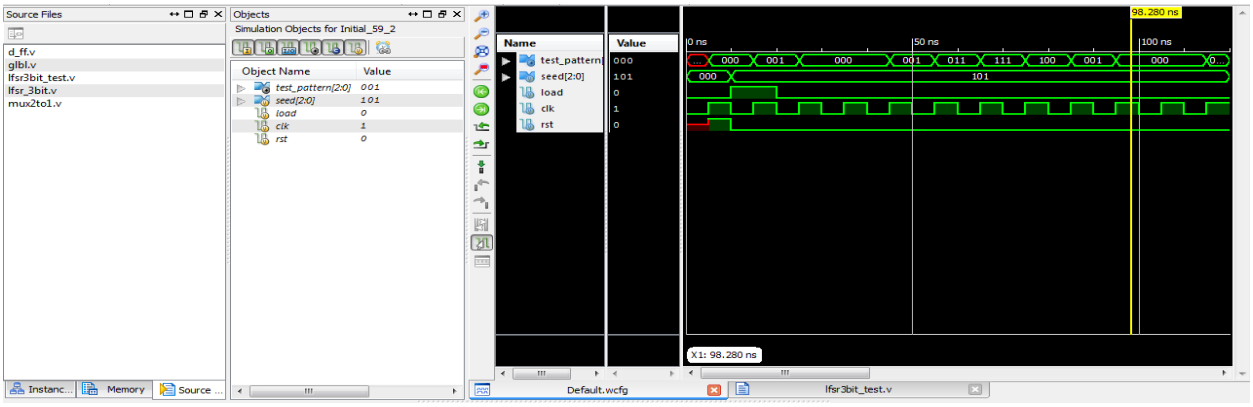
Test Pattern Sequence:

S. No	Q[2]	Q[1]	Q[0]
1	1	1	1
2	0	1	0
3	1	0	0
4	0	1	1
5	0	1	1
6	1	1	1
7	1	1	0
8	1	1	1
9	0	1	0

Note: Pattern 001 is replaced by 011. (Occurrence of 000 and 101 pattern is not possible)

Seed Value: 101 (Never appears at the output)

Weighted LFSR (With Probability of Number of 1s = 0.125)



International Journal of Recent Research in Science, Engineering and Technology

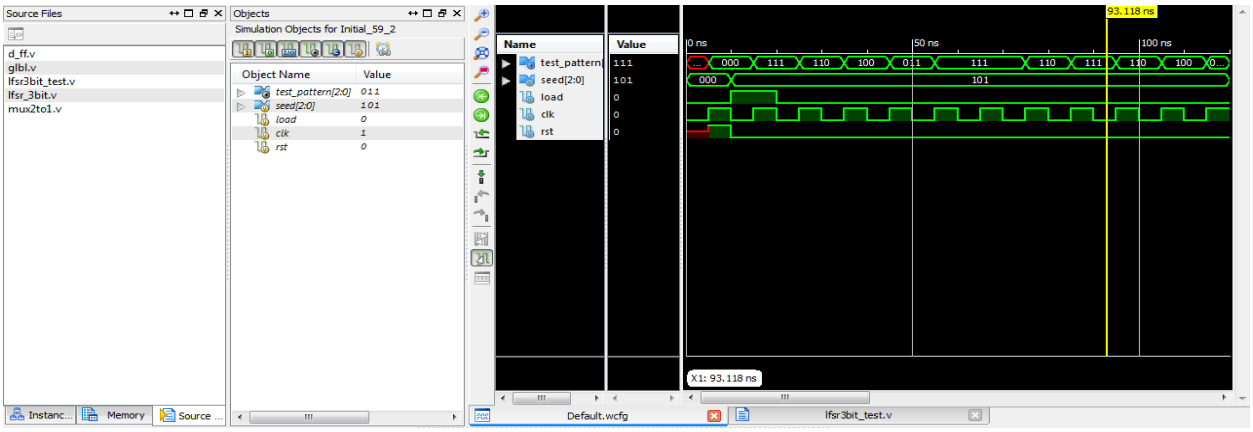
Vol. 1, Issue 1, April 2015

Test Pattern Sequence:

S. No	Q[2]	Q[1]	Q[0]
1	0	0	1
2	0	0	0
3	0	0	0
4	0	0	1
5	0	1	1
6	1	1	1
7	1	0	0
8	0	0	1
9	0	0	0

Note: Pattern 110, 010 and 101 is replaced by 000. Seed Value: 101

Weighted LFSR (With Probability of Number of 1s = 0.875)



International Journal of Recent Research in Science, Engineering and Technology

Vol. 1, Issue 1, April 2015

Test Pattern Sequence:

S. No	Q[2]	Q[1]	Q[0]
1	1	1	1
2	1	1	0
3	1	0	0
4	0	1	1
5	1	1	1
6	1	1	1
7	1	1	0
8	1	1	1
9	1	1	0

Note: Pattern 001, 010 and 101 is replaced by 111. Seed Value: 101

V. Conclusion

The *International Technology Roadmap for Semiconductors* (ITRS) published by the Semiconductor Industry Association (SIA) have shown the need to reduce power consumption during test of digital and memory designs. This need is triggered by the fact that power dissipation during test mode is about twice than that of the normal mode operation of the chip. In order to reduce the area and power consumption in the test circuitry various low power LFSR architectures have been proposed over the past decade. This paper has compared some of the low power LFSR architectures for Logic Built-in Self Test and their simulation results are verified using Xilinx ISE simulator. These low power LFSR structures are general and can be applied to almost all Test Pattern Generators.

International Journal of Recent Research in Science, Engineering and Technology

Vol. 1, Issue 1, April 2015

VI. References:

[1] N. H. E. Weste and K. Eshraghian. 1994. Principles of CMOS VLSI Design- A System Perspective 2nd Ed. Addison Wesley.
[**2**] M. Abramovici, M. A. Breuer, and A. D. Friedman. 2006. Digital Systems Testing and Testable Design. Jaico Publishing House, India.

[**3**] P. Girard, L. Guiller, C. Landrault, S. Pravossoudovitch, H. -J. Wunderlich, "A modified Clock Scheme for a Low Power BIST Test Pattern Generator," in Proc. *VLSI Test Symp. (VTS'01)*, pp. 306-311, 2001.

[**4**] P. Girard. 2002. Survey of low power testing of vlsi circuits. IEEE Design and Test of Computers, 19, 3, 80–90.

[**5**] Neelam R. Prakash, Akash, "Clock Gating for Dynamic Power Reduction in Synchronous Circuits", International Journal of Engineering Trends and Technology (IJETT) - Volume4Issue5- May 2013.

[**6**] Praveen Kasunde, Dr. K B ShivaKumar, Dr. M Z Kurian, "Improved Design of Low Power TPG Using LPLFSR" International Journal of Computer & Organization Trends –Volume3 Issue4 – May 2013

[7] Seongmoon Wang, *Member, IEEE* and Sandeep K. Gupta "DS-LFSR: A BIST TPG for Low Switching Activity" IEEE Transactions on computer aided design of Integrated circuits and Systems, VOL. 21, NO. 7, JULY 2002

[**8**] C. Chin and E. J. McCluskey, "Weighted pattern Generation for Built-in self test", Center for reliable computing Technical report, No. 84-7, Stanford University, 1984.

[**9**] S. Wang and S. K. Gupta, "DS-LFSR: A New BIST TPG for Low Heat Dissipation," *Proc. Int'l Test Conf.*, pp. 848-857, November 1997.

[10] Pomeranz, I., and S. M. Reddy. 3-Weight Pseudo-Random Test Generation Based on a Deterministic Test Set. IEEE Trans. On Computer-Aided Design, pp. 1050-1058, July 1993.
[**11**] S. Wang and S. K. Gupta, "LT-RTPG: A New Test-Per-Scan BIST TPG for Low Heat Dissipation," *Proc. Int'l Test Conf.*, pp. 85-94, September 1999.

[**12**] X. Zhang and K. Roy, "Peak Power Reduction in Low Power BIST," in Proc. *Int. Symp. on Quality Elect. Design (ISQED'01)*, pp. 425-432, 2001.

[**13**] L. Benini, A. Bogliolo, and G. D. Micheli, "A survey of design techniques for system-level dynamic power management," IEEE Trans. Very Large Scale Integr. (VLSI) Syst., vol. 8, no. 3, pp. 299–316, Jun. 2000.
[14] AlShaibi, M.F., and C. R. Kime. Fixed-biased Pseudo-random Built in Self-test for Random Pattern Resistant Circuits. Proc.of International Test Conf., pp. 929-938, 1994.