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GENERATOR FOR LOW POWER BIST WITH PRESELECTED SWITCHING

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ABSTRACT: In this paper presents a new pseudorandom test pattern generator with preselected switching activity is showed. It is comprised of a linear finite state machine (a linear feedback shift register) driving an appropriate phase shifter and armed with a number of features that allows this device to produce binary sequences with low toggling or switching rates while preserving test coverage achievable by the best-to-date conventional BIST-based PRPGs with negligible impact on test application time while on-line and off-line testing.

KEYWORDS: **Pseudorandom test pattern generator, Toggling, Switching, BIST, PRPG.**

I. INTRODUCTION

The various forms of embedded test are increasingly viewed as essential to reduce test cost. Among them, scan testing has gained broad acceptance as a reliable solution. However, due to the high data activity associated with scan-based test operations, a circuit under test can dissipate much more power than it was designed to function under. With overstressing devices beyond the mission mode, reductions in the operating power of ICs in a test mode have been of concern for years. A full-toggle scan pattern may draw several times the typical functional mode power, and this trend continues to rise, particularly over the mission mode's peak power. This power-induced over-test may result in thermal issues, voltage noise, power droop, or excessive peak power over multiple cycles which, in turn, cause a yield loss due to instant device damage, severe decrease in chip reliability, shorter product lifetime, or a device malfunction because of timing failures following a significant circuit delay increase, for example. Abnormal switching activity may also cause fully functional chips to fail during testing because of phenomena such as IR-drop, crosstalk, or di/dt problem. Numerous schemes for power reduction during scan testing have been devised [8]. Among them there are solutions specifically proposed for built-in self-test (BIST) to keep the average and peak power below a given threshold. For example, the test power can be reduced by preventing transitions at memory elements from propagating to combinational logic during scan shift. This is achieved by inserting gating logic between scan cell outputs and logic they drive [4], [9]. During normal operations and capture, this logic remains transparent. Gated scan cells are also proposed in [2] and [20]. A synergistic test power reduction method of [21] uses available on-chip clock gating circuitry to selectively block scan chains while employing test scheduling and planning to further decrease BIST power in the Cell processor. A test vector inhibiting scheme of [5] masks test patterns generated by an LFSR as not all produced vectors, often very lengthy, detect faults. Elimination of such tests can reduce switching activity with no impact on fault coverage.

The advent of low-transition test pattern generators has added a new dimension to power aware BIST solutions [3],[11], [15]. A device presented in [19] is comprised of an LFSR feeding scan chains through biasing logic and T-type flip-flop. Since this flip-flop holds the previous value until its input is asserted, the same value is repeatedly scanned into scan chains until the value at the output of biasing logic (e.g., a k-input AND gate) becomes 1. Depending on k, one can significantly reduce the number of transitions occurring at the scan chain inputs. A dual-speed LFSR of [18] consists of two LFSRs driven by normal and slow clocks, respectively. The switching activity is reduced at the circuit inputs connected to the slow-speed LFSR, while the whole scheme still ensures satisfactory fault coverage. Mask patterns are used in [14] to mitigate the switching activity in LFSR-produced patterns, whereas a bit swapping of [1] achieves the same goal at the primary inputs of CUT. A gated LFSR clock of [6] allows one to activate only half of

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LFSR stages at a time, thus reducing power consumption, as only half of the circuit inputs change every cycle. A scheme that com-bines the low transition generator of [19] (handling easy-to-detect faults) with a 3-weight PRPG (deployed to detect random pattern resistant faults) can also be used to reduce switching activity during BIST, as demonstrated in [17]. The schemes of [10], [13], and [16] suppress transitions in LFSR-generated sequences by either statistical monitoring or injecting intermediate and highly correlated patterns. Finally, a random single-input change generator can produce low power patterns in a parallel BIST environment, as shown in [7].

As the BIST power consumption can easily exceed the maximum ratings when testing at speed, scan patterns must be shifted at a programmable low speed, and only the last few cycles and the capture cycle are applied at the maximum frequency. In the burst-mode approach presented in [12], typically five consecutive lock cycles are used. The first four cycles serve shifting purposes, whereas the last one is designated for capture. The objective is to stabilize the power supply before the last shift and capture pulses are applied, which are critical for at - speed tests. To reduce the voltage droop related to a higher circuit activity, a burst clock controller slows down some of the shift cycles. It allows a gradual increase of the circuit activity, thereby reducing the di/dt effect. The controller can gate the shift clocks, depending on the needs for gradual warming up of the circuit.

In this paper, we propose a new pseudorandom test pat-tern generator (PRPG) for low power BIST applications. The generator is aimed at reducing the switching activity during scan loading due to its preselected toggling (PRESTO) levels. It can assume a variety of configurations that allow a given scan chain to be driven either by PRPG itself or by a constant value fixed for a given period of time. The PRESTO generator allows loading scan chains with patterns having low transition counts, and thus significantly reduced power dissipation.

II. BASIC ARCHITECTURE

Figure 1 illustrates the basic structure of a PRESTO generator. It consists of an *n*-bit conventional PRPG connected with a phase shifter feeding scan chains. Linear feedback shift register or a ring generator can implement PRPG. More importantly, however, *n* hold latches are placed between the PRPG and the phase shifter. Each hold latch is individually controlled through a corresponding stage of an *n*-bit shift register. As long as its enable input is asserted, the given latch is transparent for data going from the PRPG to the phase shifter, and it is said to be in the *toggle mode*. When the latch is disabled, it captures and saves, for a number of clock cycles, the corresponding bit of PRPG, thus feeding the phase shifter (and possibly certain scan chains) with a constant value. Now, it is in the *hold mode*. It is worth noting that each phase shifter output is obtained by XORing out-puts of three different hold registers. Thus, every scan chain remains in a low-power mode provided only disabled hold latches drive the corresponding phase shifter output.

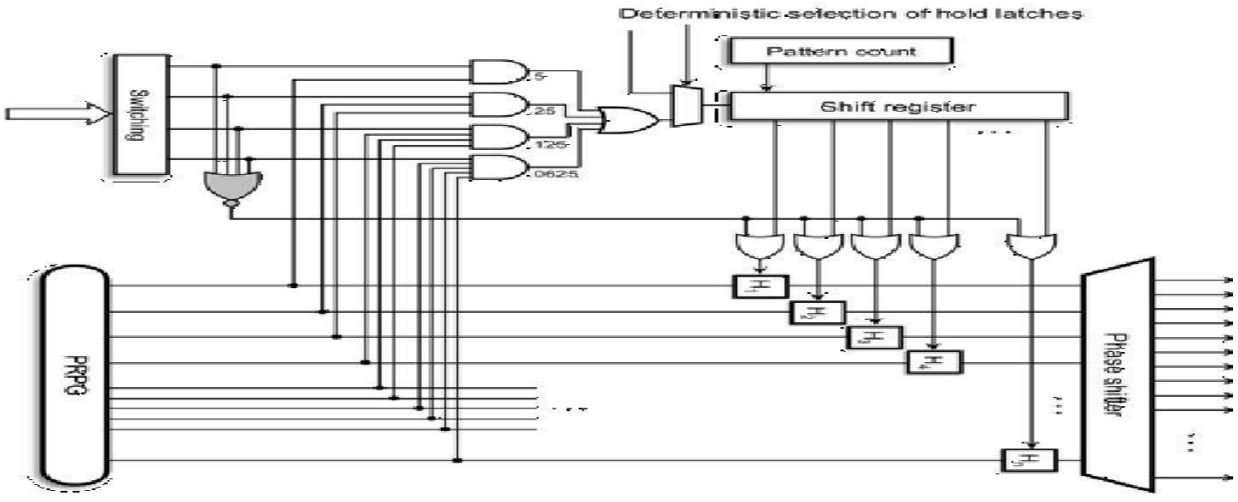

Fig. 1 The basic architecture of PRESTO generator

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As mentioned above, the shift register controls the hold latches. Its content comprises 0s and 1s shifted-in one bit per test pattern. The 1s indicate latches in the toggle mode and thus transparent for data arriving from the PRPG. Their fraction determines a scan switching activity. Yet one should recall that only scan chains driven exclusively through disabled hold latches will receive constant values. The enable signals stored in the shift register are produced in a probabilistic fashion. The scheme of Fig. 1 uses the PRPG with a programmable set of weights to output weighted pseudorandom samples. The weights are determined by four AND gates producing a logical 1 with the probability of 0.5, 0.25, 0.125, and 0.0625, respectively. The OR gate allows choosing probabilities beyond simple powers of 2. A 4-bit register *Switching* is employed to activate AND gates, and allows selecting a user -defined level of desired switching activity. For example, if one enters the switching code 0100, then, on the average, 25% of the shift register stages will be set to 1, and thus 25% of hold latches will be enabled. Given the phase shifter architecture, one can assess then the amount of scan chains receiving constant values, and thus the expected toggling ratio.

An additional 4-input NOR gate (in gray) detects the switching code 0000, which is used to switch the low power functionality off. The content of the shift register can also be selected in a deterministic manner due to a multiplexer placed in the front of the serial input of the register. It is worth noting that when working in the weighted random mode, the switching level selector ensures statistically stable content of the shift register in terms of the amount of 1s it carries. As a result, roughly the same fraction of scan chains will stay in the low power mode, though a set of actual low toggling chains will keep changing from one test pattern to another. It will correspond to a certain level of toggling in the scan chains. With only 15 different switching codes, however, the available toggling granularity may render this solution too coarse to be always acceptable. The next section presents additional features that make the PRESTO generator fully operational in a wide range of desired switching rates.

III.FULLY OPERATIONAL GENERATOR

Much higher flexibility in forming low-toggling test pat-terns can be achieved by deploying a scheme presented in Fig. 2. Essentially, while preserving the operational principles of the basic solution, this approach splits up a shifting period of every test pattern into a sequence of alternating hold and toggle intervals. To move the generator back and forth between these two states, we use a basic T -type flip-flop that switches whenever there is a 1 on its data input. If it is set to 0, the generator enters the hold period with all latches temporarily disabled regardless of the shift register con-tent. This property can be crucial in SoC designs where only a single scan chain crosses a given core, and its abnormal toggling may cause locally unacceptable heat dissipation that can only be reduced due to temporary hold periods. To make it work, it first requires placing AND gates on the shift register outputs to allow freezing of all phase shifter inputs. If the T flip-flop is set to 1 (the toggle period), then the latches enabled through the shift register can pass test data moving from the PRPG to the scan chains.

How long it takes to stay either in the hold mode or in the toggle mode is decided by two additional user-defined parameters kept in 3-bit *Hold* and *Toggle* registers, respectively. In order to terminate either mode, a 1 must occur on the T flip-flop input. This weighted pseudorandom signal is produced by a module *Encoder* H/T based on the content of seven different stages of the original PRPG, as shown in Fig. 3. Depending on the control code provided by either the Toggle register or the Hold register, the encoder output can be asserted with the probability ranging from 2^{-1} to 2^{-7}. Moreover, the control code 000 causes the encoder to assume the high output unconditionally. This property can be used to terminate deterministically a given period (hold or toggle) within a single clock cycle state. They will remain in this state until another 1 occurs on the encoder output. The random occurrence of this event is related to the content of the Hold register that determines The actual results are presented in Tables II and III for the industrial designs of Table I. In all experiments reported in the remaining part of this section, we have used the PRESTO generator with a 32-bit ring generator producing 128K pseudorandom test patterns in a low power mode. Table II is vertically partitioned into three sections corresponding to the following target toggling rates: 5%, 10%, and 15%. Four different switching activity codes as well as appropriate parameters H and T decide on approximate values of switching rates, as shown in the previous sections. The actual toggling observed during the experiments for our three target rates ended up within the following intervals: (14.16 – 16.51), (9.12 – 10.56) with a few exceptions going down to 7%, and (3.92 – 5.88), respectively. All the PRESTO setup data deployed during the experiments are displayed in the table header. The columns of Table II list the fault coverage for successive test cases. As can be seen, the resultant fault coverage remains

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close to the reference coverage reported in Table I, while the switching activity is significantly reduced in all examined cases. Note that several experimental results indicate higher fault coverage if the scan chains receive the low toggling patterns rather than conventional pseudorandom vectors. Even if this is a circuit-specific feature, it nevertheless appears to be the case across several designs.

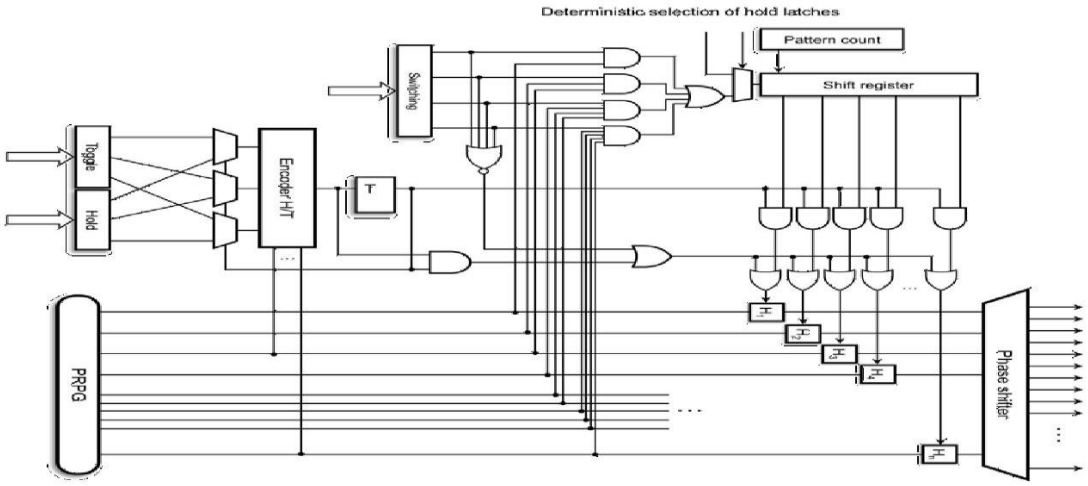

Fig.2 Full version of PRESTO

The objective of the analysis summarized in Table III was to determine the impact of our low power test generator performance on a pattern count. Alternatively, we would like to assess how long it takes to match fault coverage of purely pseudorandom test with vectors produced by the PRESTO generator. Let $L(p)$ and $R(p)$ denote fault coverage obtained by applying p low toggling and purely random test patterns, respectively. Clearly, there are two possible scenarios: either $L(p) < R(p)$ or $L(p) > R(p)$. In the first case, we can assess a pseudorandom test length q to get fault coverage $L(p)$, where $q < p$. The other case is symmetrical: we need to find the number of low power test patterns r that suffice to match fault coverage $R(p)$, where $r < p$. The entries of Table III, corresponding directly to those of Table II, are ratios v that (depending on one of the above scenarios) are either equal to p/q or r/p. Clearly, $v < 1$ indicates cases where a low power test is shorter than its random counterpart. If $v > 1$, then the presented values are indicative of how many additional low power test patterns must be applied to obtain $R(p)$. Table III two horizontal segments present results for two values of p: 16K and 128K. As an example, the entry 3.01 for design D1, 16K vectors, and WTM = 10% indicates that the resultant fault coverage due to 16K low toggling test patterns can be reached three times faster by using pseudorandom tests. On the other hand, the entry 0.52 for design D6 and otherwise similar conditions indicates that low power tests can offer the same fault coverage as that of 16K random patterns in approximately half shorter test time. One may also observe that for some test cases the ratio v is quite large. It occurs for aggressively low toggling rates (such as 5% in the table) and in some designs where certain groups of faults are much more difficult to detect by means of test patterns with relatively low diversity of binary sequences.

IV.CONCLUSION

This paper presents architecture of a low power pseudorandom test pattern generator with programmable features that allow selection of wide range of user-defined toggling rates. Experimental results for scan -based BIST applications include both Monte Carlo-derived switching activity numbers as well as fault coverage statistics for several industrial designs. Comparisons with conventional PRPGs clearly indicate that the PRESTO generator can reduce switching activity down to single-digit percentage numbers while virtually preserving original test coverage, and even visibly reducing, in some test cases, test pattern counts.

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TABLE I. FAULT COVERAGE – 1280 LOW SWITCHING TEST PATTERNS

		WTM " 5%				WTM " 10%				WTM " 15%		
	S:0001	S:0010	S:0100	S:1000	S:0001	S:0010	S:0100	S:1000	S:0001	S:0010	S:0100	S:1000
	H:4 T:1	H:6 T:3	H:5 T:3	H:6 T:5	H:4 T:2	H:6 T:4	H:4 T:4	H:2 T:3	H:3 T:2	H:3 T:3	H:3 T:5	H:1 T:1
D1	89.95	90.00	89.99	89.98	90.98	90.71	91.20	91.08	91.62	91.68	91.76	90.98
D2	85.57	85.51	86.34	86.32	87.96	87.46	88.88	88.70	89.43	89.85	89.63	88.21
D3	85.97	85.68	86.44	85.63	89.91	88.35	90.30	89.82	91.84	92.07	91.41	89.35
D4	81.91	81.40	82.04	81.65	84.07	83.33	84.55	84.55	85.24	85.57	85.39	84.07
D5	88.63	87.45	88.36	87.37	89.72	88.83	89.87	90.00	90.35	90.41	90.22	89.96
D6	90.05	89.92	90.34	89.74	91.49	91.14	91.66	91.47	91.96	91.97	91.87	91.52
D7	85.62	84.67	85.46	84.50	86.23	85.31	86.29	86.11	86.12	86.17	86.47	85.60
D8	83.38	82.56	83.09	82.54	84.39	83.58	84.49	84.43	84.89	85.04	84.91	84.48

TABLE II. LOW SWITCHING TEST PATTERN COUNT VS. RANDOM VECTORS

		WTM " 5%				WTM " 10%				WTM " 15%		
	S:0001	S:0010	S:0100	S:1000	S:0001	S:0010	S:0100	S:1000	S:0001	S:0010	S:0100	S:1000
	H:4 T:1	H:6 T:3	H:5 T:3	H:6 T:5	H:4 T:2	H:6 T:4	H:4 T:4	H:2 T:3	H:3 T:2	H:3 T:3	H:3 T:5	H:1 T:1
					After 16K test patterns							
D1	4.72	6.25	5.81	6.58	2.94	4.31	2.98	3.01	2.23	1.91	1.79	2.63
D2	13.16	17.86	13.16	14.71	6.41	9.62	4.63	4.90	3.62	2.84	3.05	5.10
D3	5.81	8.33	7.35	8.93	3.33	5.43	3.33	3.73	2.12	2.02	2.48	3.33
D4	6.58	8.62	7.35	8.93	3.42	5.21	3.25	3.25	1.84	1.77	1.95	2.81
D5	13.16	27.78	17.86	27.78	6.41	15.63	6.41	4.81	2.23	2.17	4.10	3.97
D6	1.08	1.59	1.34	2.29	0.46	0.85	0.58	0.52	0.29	0.28	0.46	0.57
D7	1.45	2.40	1.48	2.78	1.04	1.69	0.96	0.94	0.85	0.76	0.83	1.01
D8	2.23	3.38	2.81	4.03	1.58	2.55	1.66	1.53	1.14	1.12	1.28	1.32
					After 1280 test patterns							
D1	6.39	6.35	6.39	6.39	3.19	3.80	2.59	2.84	1.91	1.80	1.66	3.19
D2	24.39	28.57	19.61	19.61	9.01	12.20	5.45	5.83	4.03	2.75	3.34	7.87
D3	10.87	11.49	9.80	11.63	4.27	6.37	3.75	4.41	2.10	1.86	2.53	4.96
D4	11.05	13.51	10.47	12.35	3.59	5.54	2.69	2.69	1.64	1.25	1.45	3.59
D5	25.97	51.28	32.26	54.05	9.13	22.22	7.35	5.88	2.24	1.98	3.44	6.49
D6	2.28	2.44	1.81	2.79	0.59	0.96	0.47	0.55	0.22	0.18	0.26	0.51
D7	0.90	1.47	0.95	1.62	0.65	1.04	0.64	0.69	0.67	0.63	0.57	0.86
D8	2.42	3.95	2.91	4.00	1.12	2.11	1.02	1.08	0.77	0.71	0.78	1.03

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